ECE 204 Introduction to Digital Logic Bill Nelson

Homework #7

NAME: _____ Due: 03/06/2017

Show your work. Answers without supporting work will not earn full credit.
Ignore all flip-flop sets and resets.

1. Draw a five D flip-flop Johnson counter. Do not include forbidden state detection. Assuming the flip-flops are initially all ones, show the successive states through the return to all ones.

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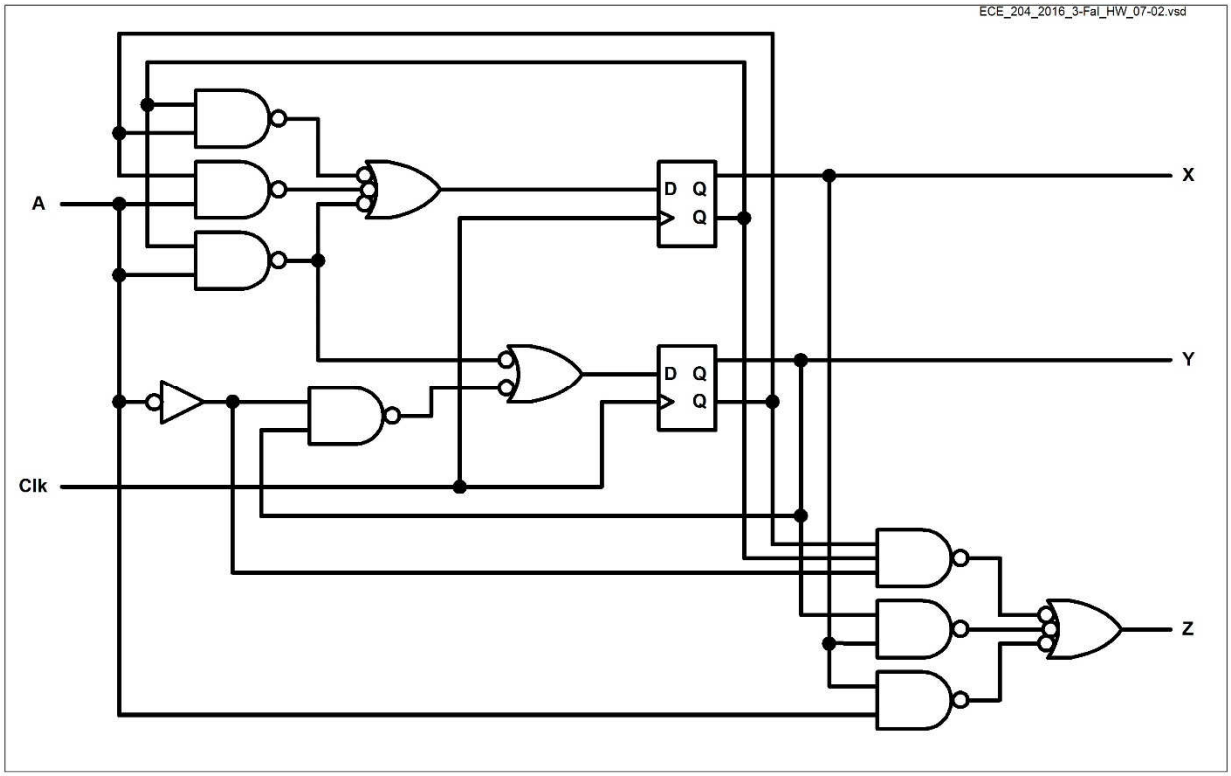
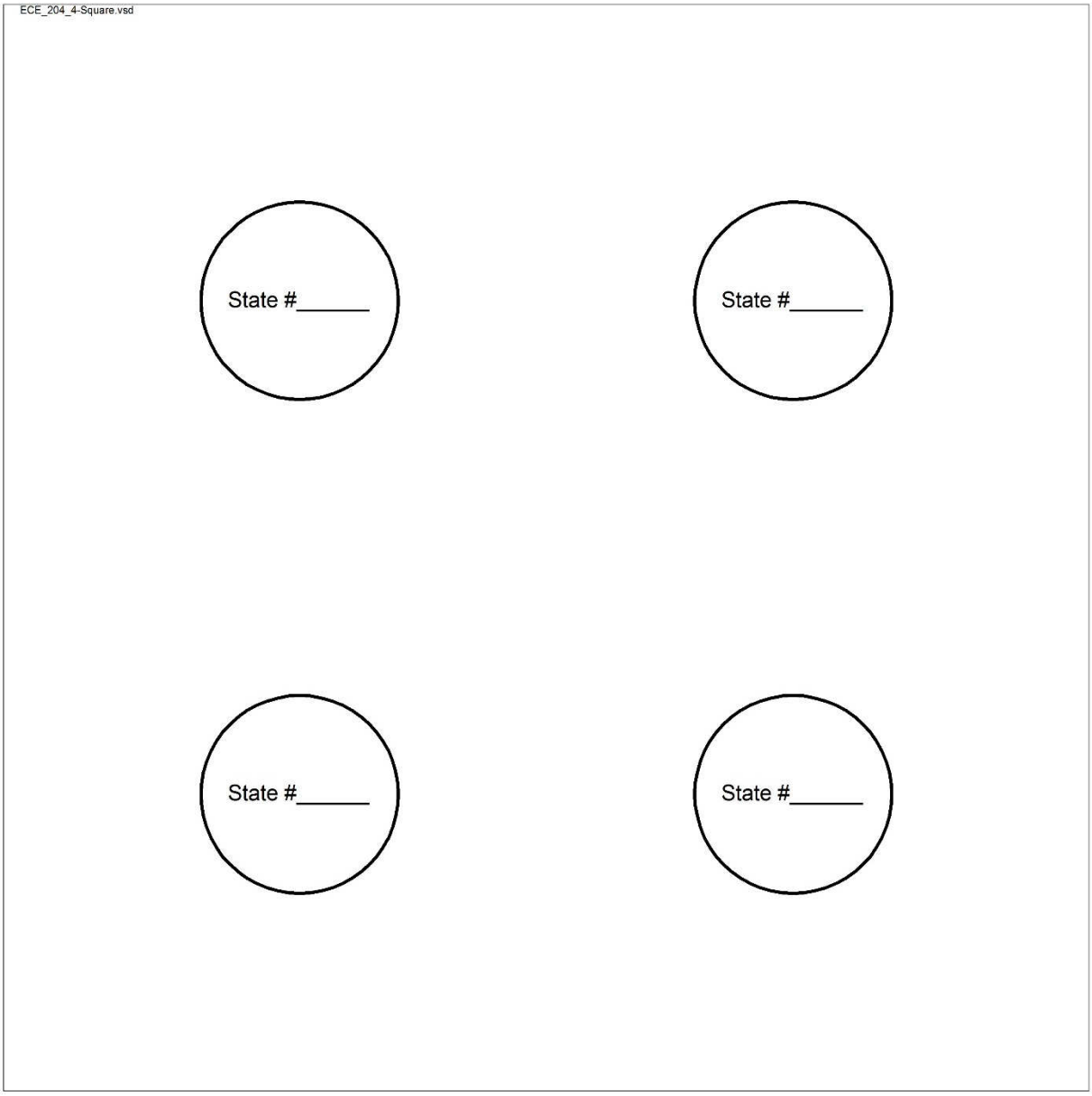
2. Given the following circuit, generate its state chart and draw its state diagram.

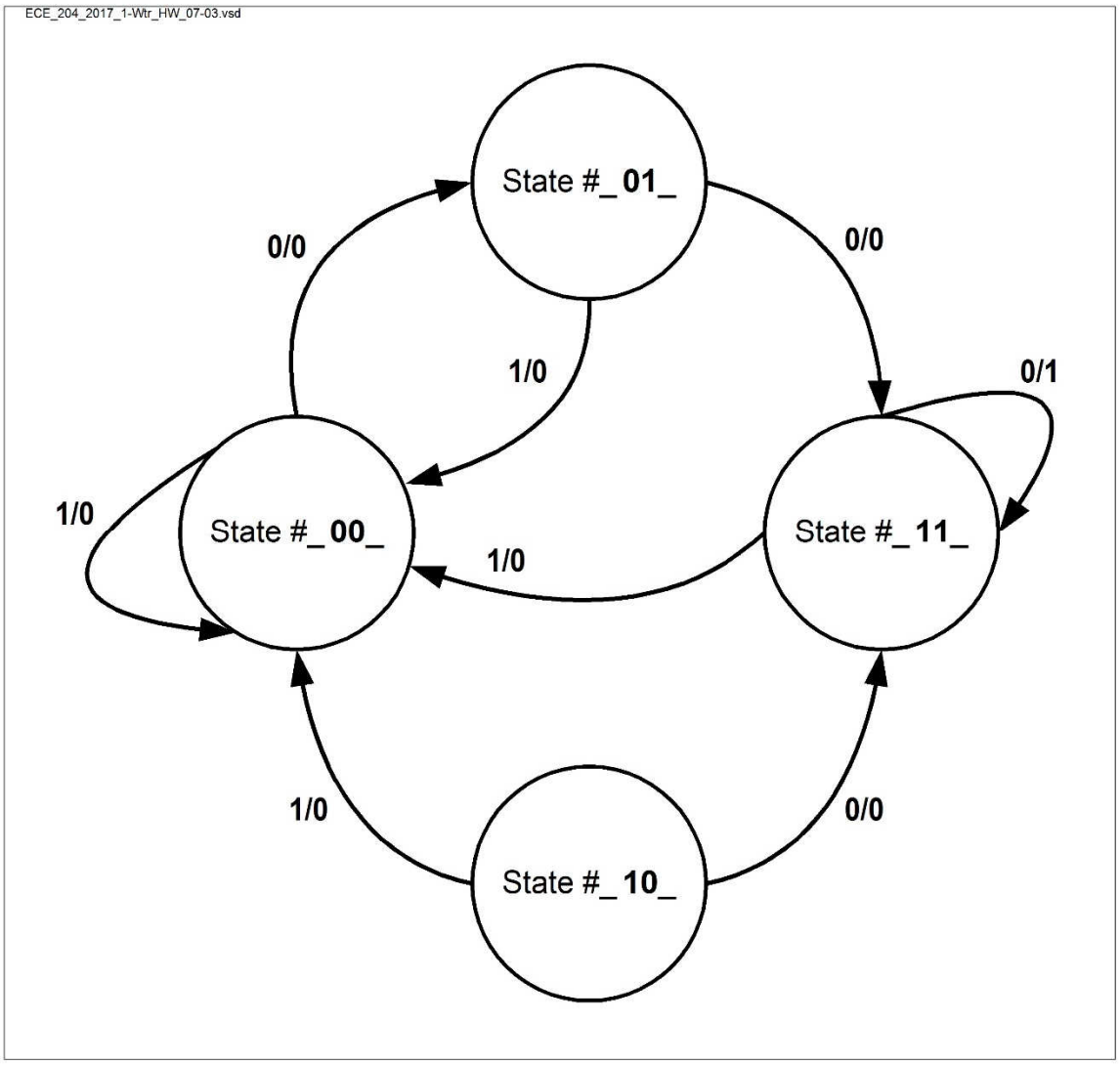


X	Y	A	X^+	Y^+	Z	D_X	D_Y
0	0	0					
0	0	1					
0	1	0					
0	1	1					
1	0	0					
1	0	1					
1	1	0					
1	1	1					

PROBLEM #2, Continued:



3. Given the following state diagram, generate the corresponding state chart including the D inputs. Also give the minimized equations for the D inputs and for the output, **B**. Let the state bits be labeled **X** and **Y**, the input **A** and the output **B**.



PROBLEM #3, Continued:

X	Y	A	X^+	Y^+	B	D_X	D_Y
0	0	0					
0	0	1					
0	1	0					
0	1	1					
1	0	0					
1	0	1					
1	1	0					
1	1	1					

X / Y A	0 0	0 1	1 1	1 0
0				
1				

X / Y A	0 0	0 1	1 1	1 0
0				
1				

X / Y A	0 0	0 1	1 1	1 0
0				
1				

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4. Complete the following partial state chart by showing the necessary ***J*** and ***K*** inputs for the flip flops. Give the minimized equations for the ***J*** and ***K*** inputs and for the output, and draw the state diagram. The state bits are **A** and **B**, the input is **C** and the output is **Z**.

A	B	C	A^+	B^+	Z	J_A	K_A	J_B	K_B
0	0	0	0	1	0				
0	0	1	1	0	1				
0	1	0	0	0	0				
0	1	1	1	1	1				
1	0	0	0	0	0				
1	0	1	1	1	1				
1	1	0	1	0	0				
1	1	1	0	1	1				

PROBLEM #4, Continued:

A / B C	0 0	0 1	1 1	1 0
0				
1				

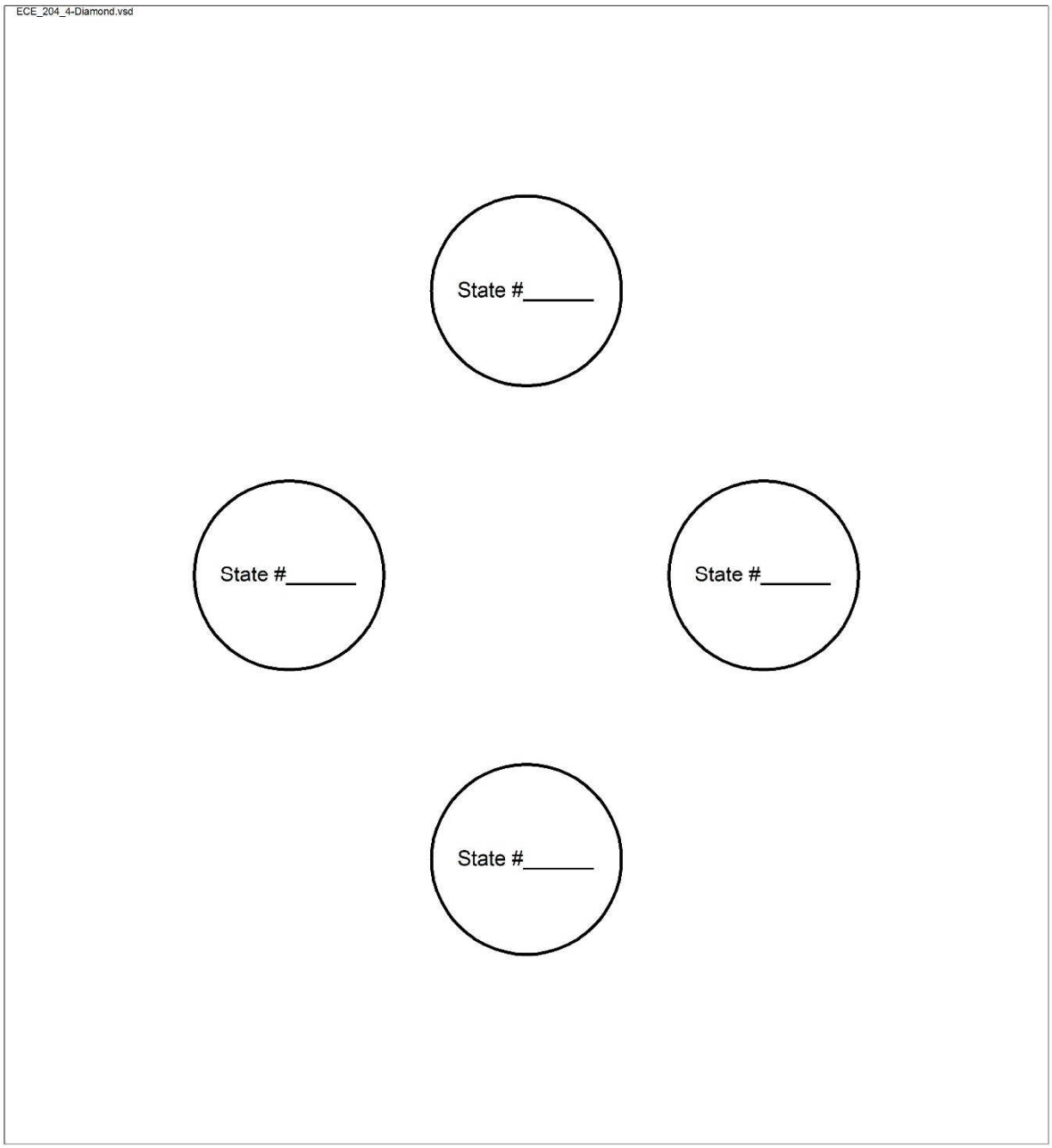
A / B C	0 0	0 1	1 1	1 0
0				
1				

A / B C	0 0	0 1	1 1	1 0
0				
1				

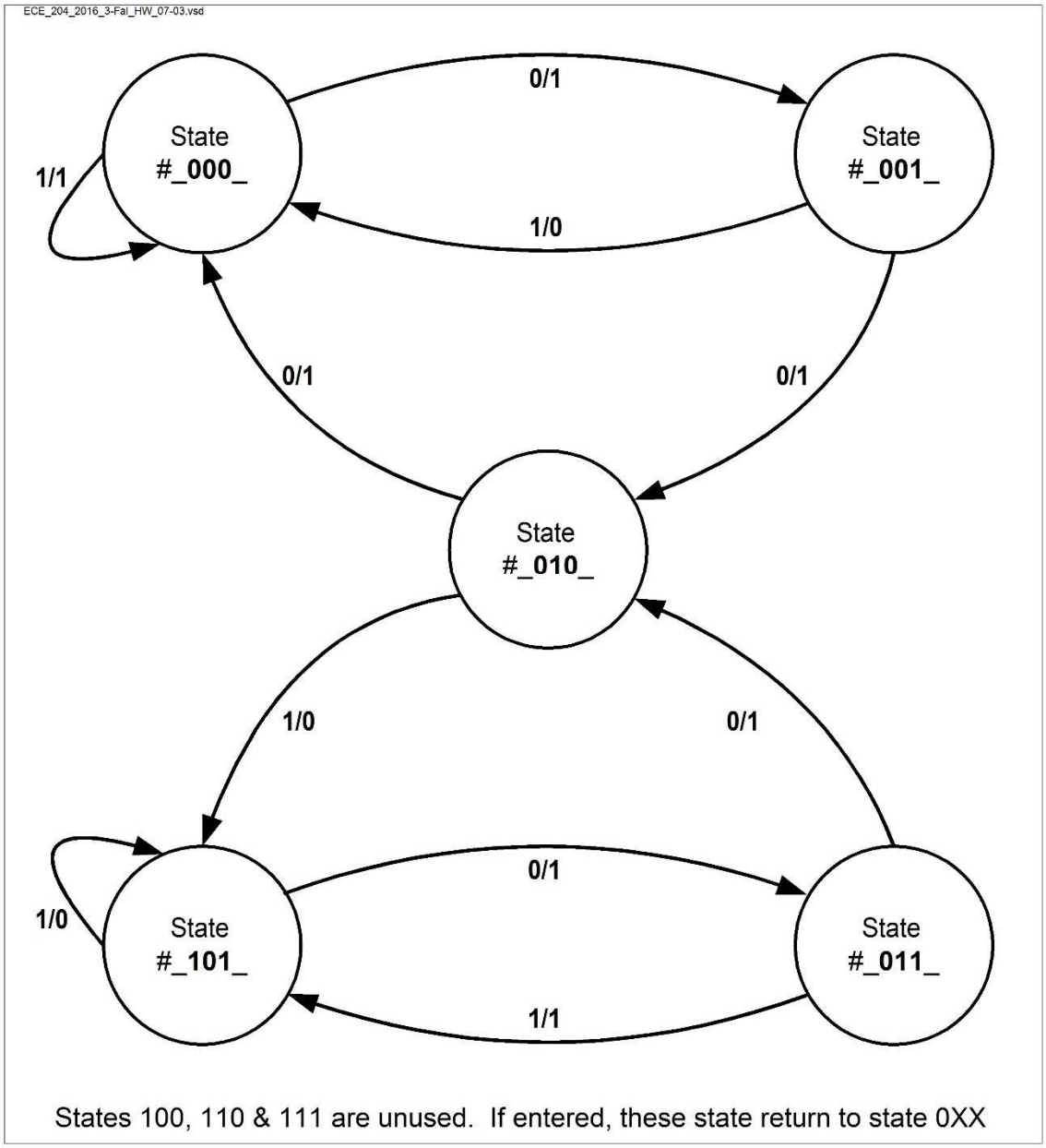
A / B C	0 0	0 1	1 1	1 0
0				
1				

A / B C	0 0	0 1	1 1	1 0
0				
1				

PROBLEM #4, Continued:



5. Given the following state diagram, generate the corresponding state chart including the necessary ***J*** and ***K*** inputs. Also give the minimized equations for the ***J*** and ***K*** inputs and for the output. Let the state bits be labeled **X**, **Y** and **Z**, the input **A** and the output ***f***.



PROBLEM #5, Continued:

X	Y	Z	A	X^+	Y^+	Z^+	f	J_X	K_X	J_Y	K_Y	J_Z	K_Z
0	0	0	0										
0	0	0	1										
0	0	1	0										
0	0	1	1										
0	1	0	0										
0	1	0	1										
0	1	1	0										
0	1	1	1										
1	0	0	0										
1	0	0	1										
1	0	1	0										
1	0	1	1										
1	1	0	0										
1	1	0	1										
1	1	1	0										
1	1	1	1										

XY / ZA	0 0	0 1	1 1	1 0
0 0				
0 1				
1 1				
1 0				

XY / ZA	0 0	0 1	1 1	1 0
0 0				
0 1				
1 1				
1 0				

PROBLEM #5, Continued:

XY / ZA	0 0	0 1	1 1	1 0
0 0				
0 1				
1 1				
1 0				

XY / ZA	0 0	0 1	1 1	1 0
0 0				
0 1				
1 1				
1 0				

XY / ZA	0 0	0 1	1 1	1 0
0 0				
0 1				
1 1				
1 0				

XY / ZA	0 0	0 1	1 1	1 0
0 0				
0 1				
1 1				
1 0				

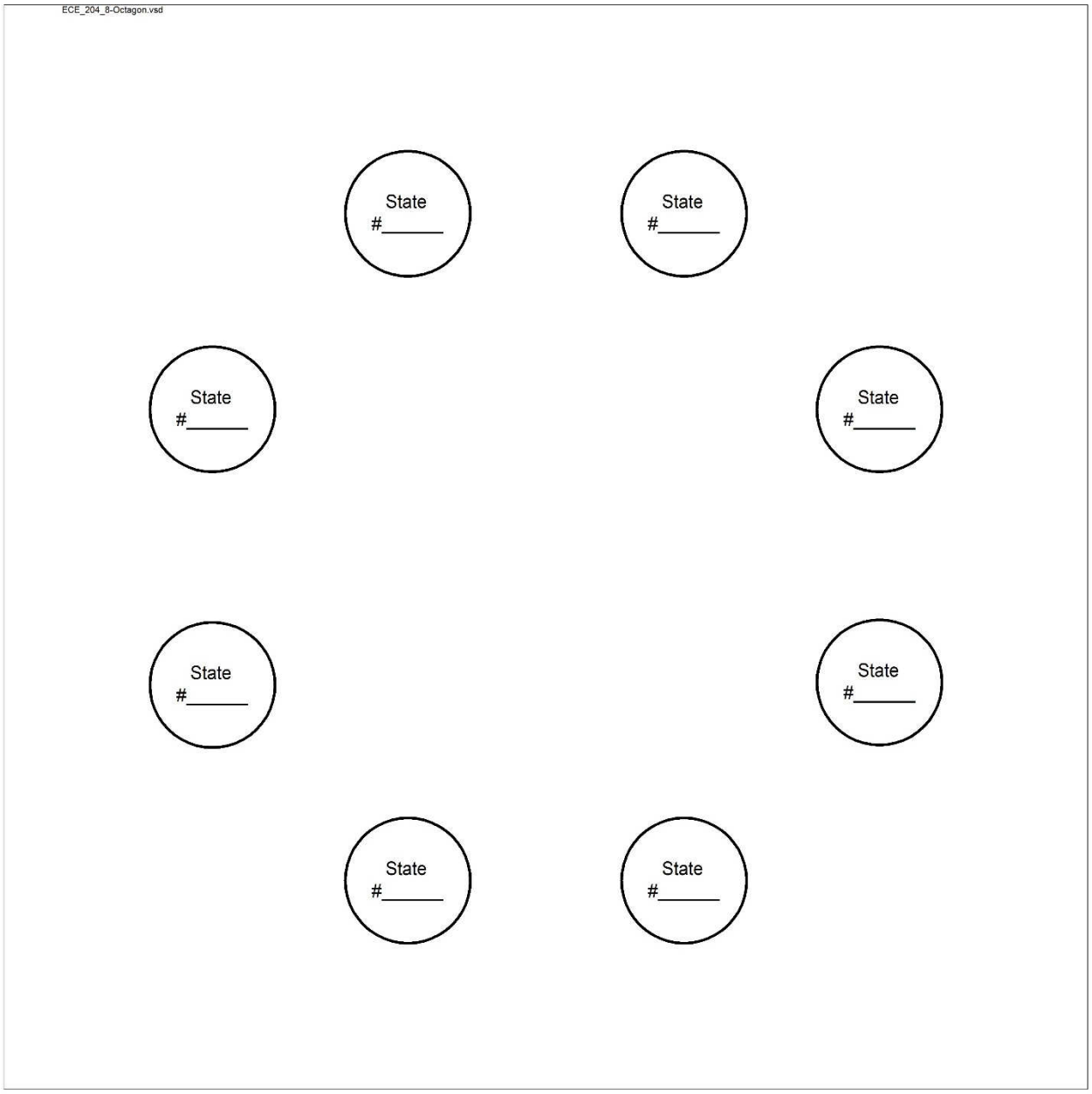
XY / ZA	0 0	0 1	1 1	1 0
0 0				
0 1				
1 1				
1 0				

6. Design an 8-state state machine counter with the following characteristics:
   - If the **e** (even) input is 1, the next state is the next even numbered state (modulo 8).
   - If the **e** input is 0, the next state is the next odd numbered state (modulo 8).
   - States are encoded using J-K flip-flops labeled **X**, **Y** & **Z** with **X** the MSB.
   - The counter has no output other than the state flip-flops.

   Give the state table, the state diagram and the minimized equations For the J and K inputs to each flip-flop.

X	Y	Z	e	X^+	Y^+	Z^+	J_X	K_X	J_Y	K_Y	J_Z	K_Z
0	0	0	0									
0	0	0	1									
0	0	1	0									
0	0	1	1									
0	1	0	0									
0	1	0	1									
0	1	1	0									
0	1	1	1									
1	0	0	0									
1	0	0	1									
1	0	1	0									
1	0	1	1									
1	1	0	0									
1	1	0	1									
1	1	1	0									
1	1	1	1									

PROBLEM #6, Continued:



PROBLEM #6, Continued:

XY / Ze	0 0	0 1	1 1	1 0
0 0				
0 1				
1 1				
1 0				

XY / Ze	0 0	0 1	1 1	1 0
0 0				
0 1				
1 1				
1 0				

XY / Ze	0 0	0 1	1 1	1 0
0 0				
0 1				
1 1				
1 0				

XY / Ze	0 0	0 1	1 1	1 0
0 0				
0 1				
1 1				
1 0				

XY / Ze	0 0	0 1	1 1	1 0
0 0				
0 1				
1 1				
1 0				

XY / Ze	0 0	0 1	1 1	1 0
0 0				
0 1				
1 1				
1 0				

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7. Draw a five D flip-flop PN counter using an XOR and taps at stages 3 and 5. Do not include forbidden state detection. Show the first 12 successive states assuming the initial state is {1,0,0,0,1}.