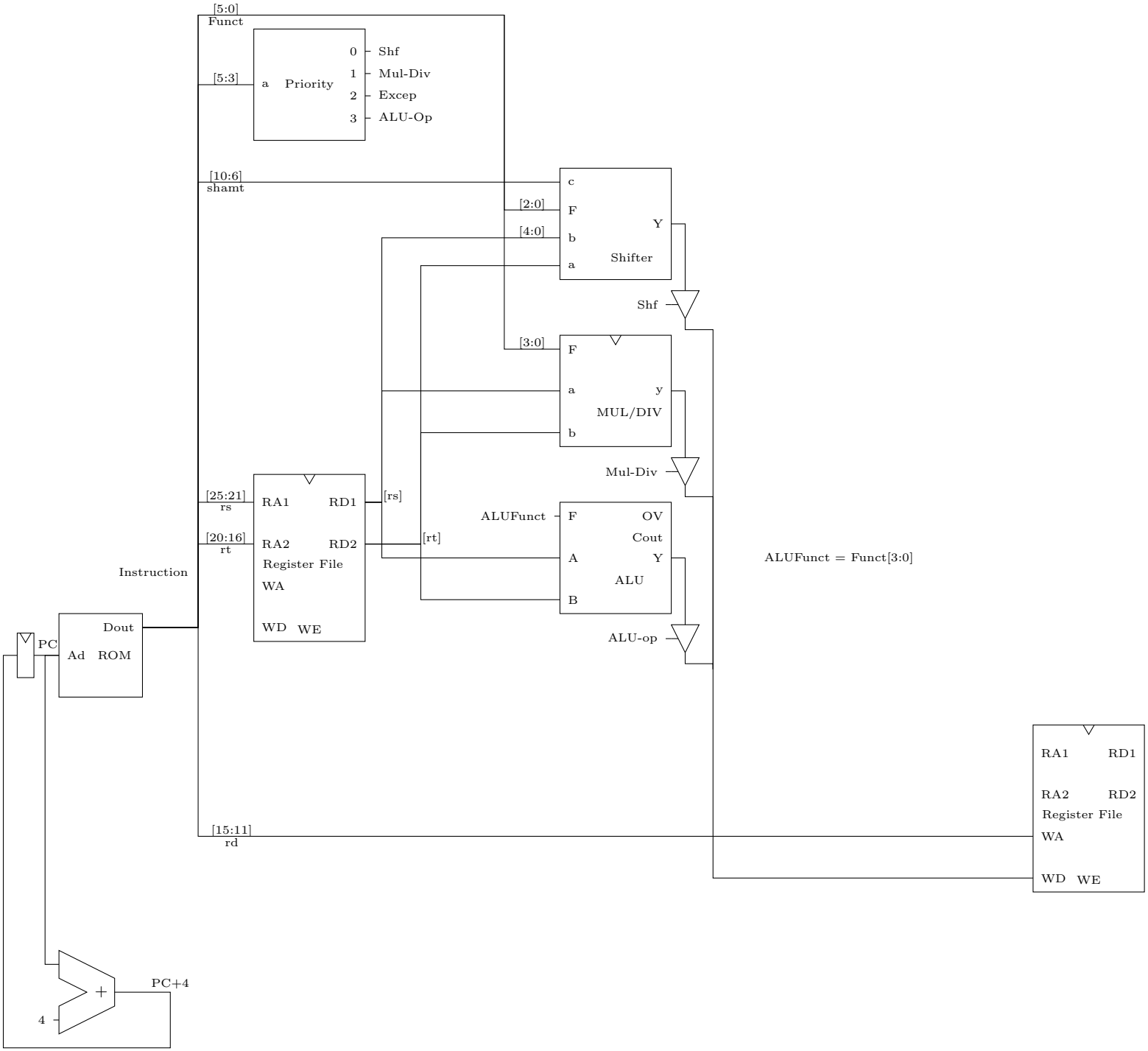
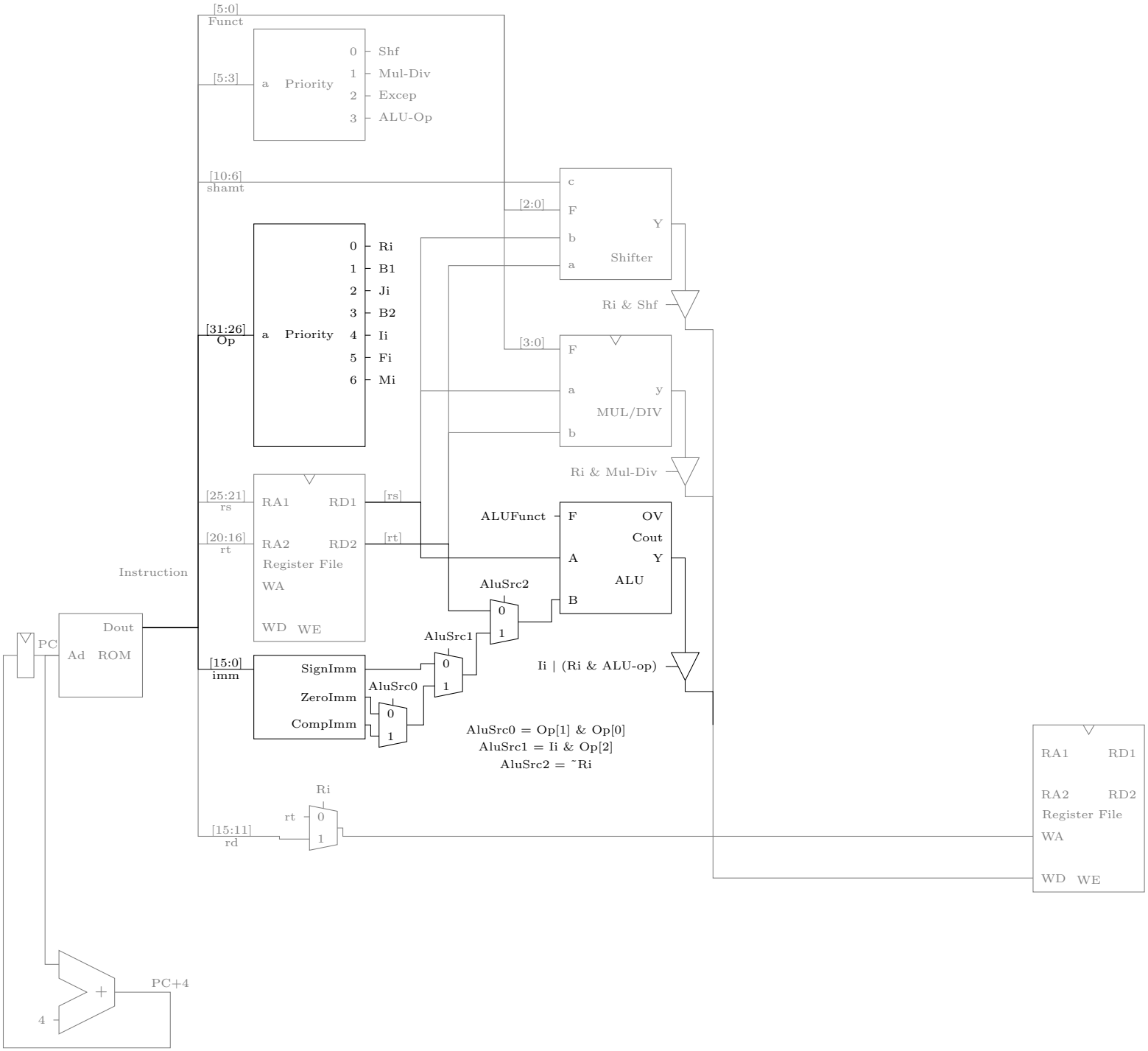
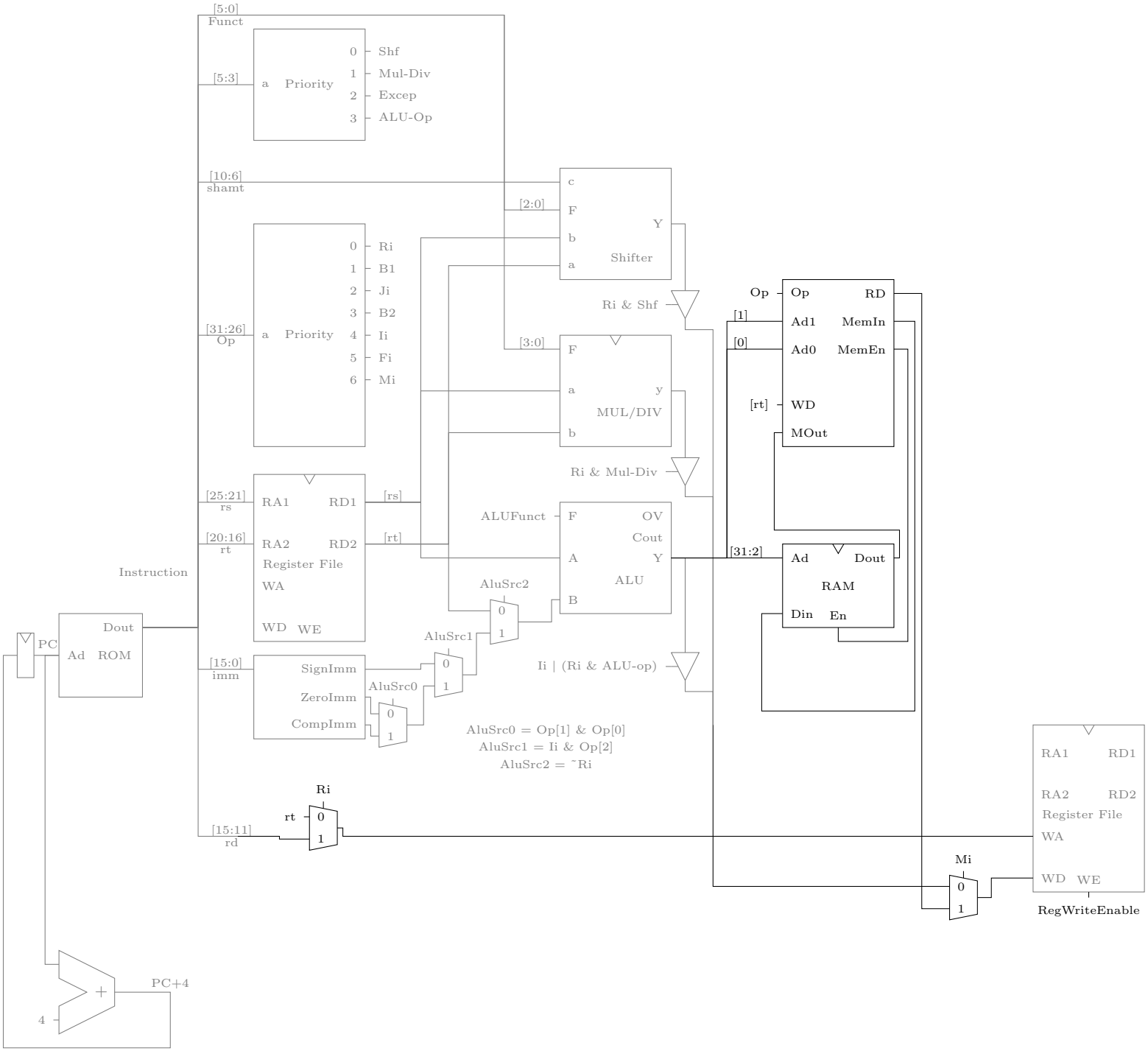
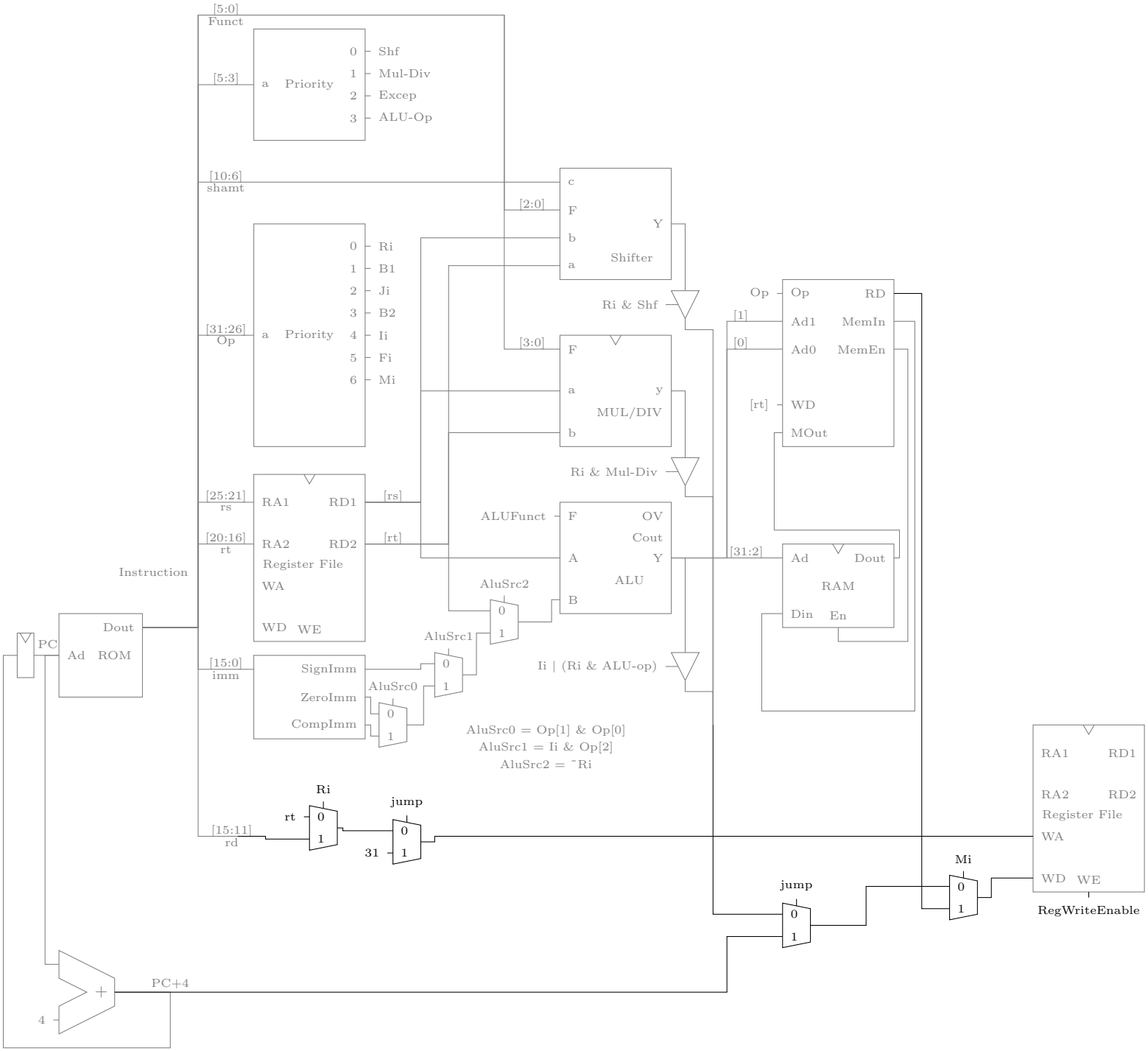
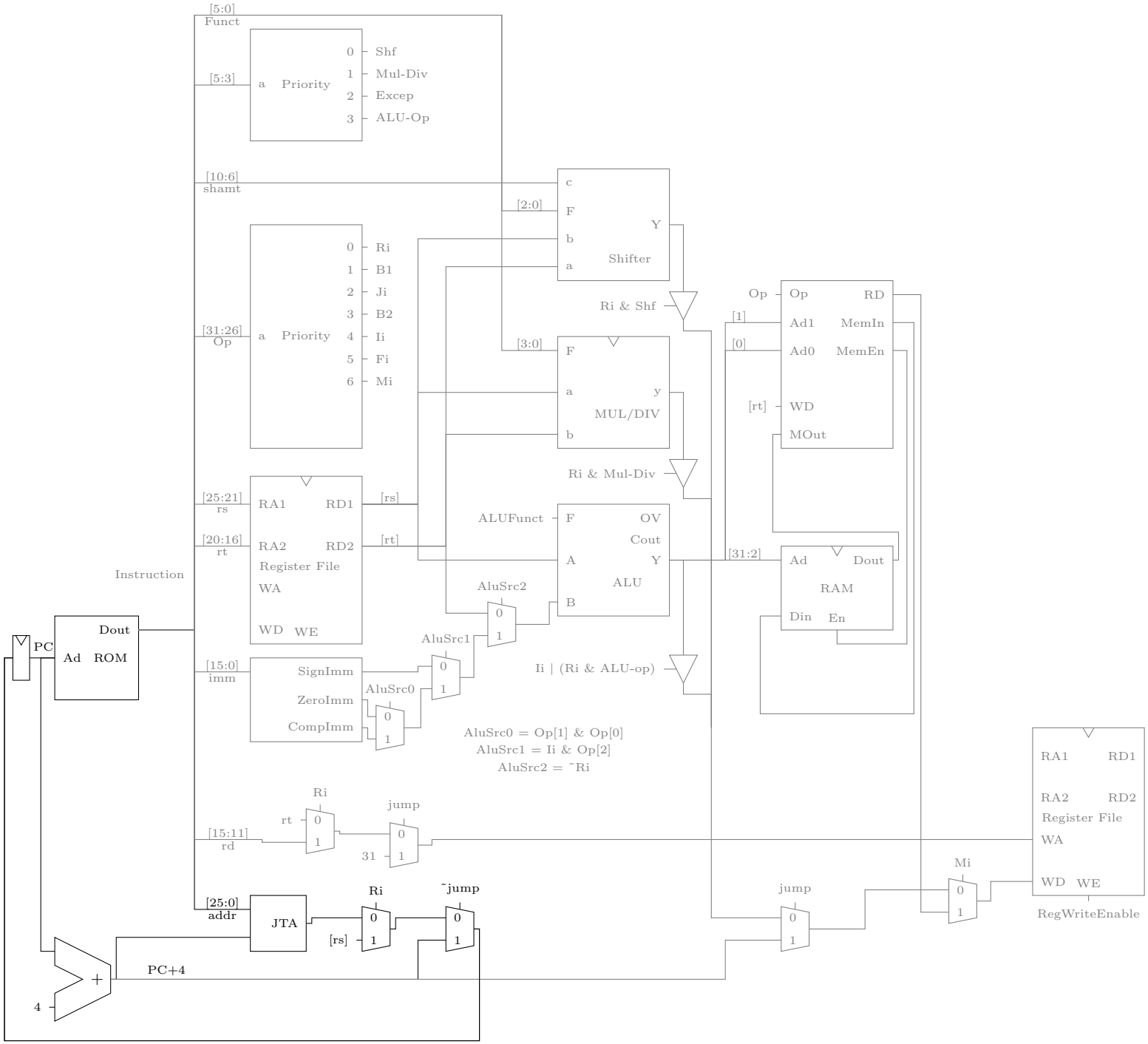
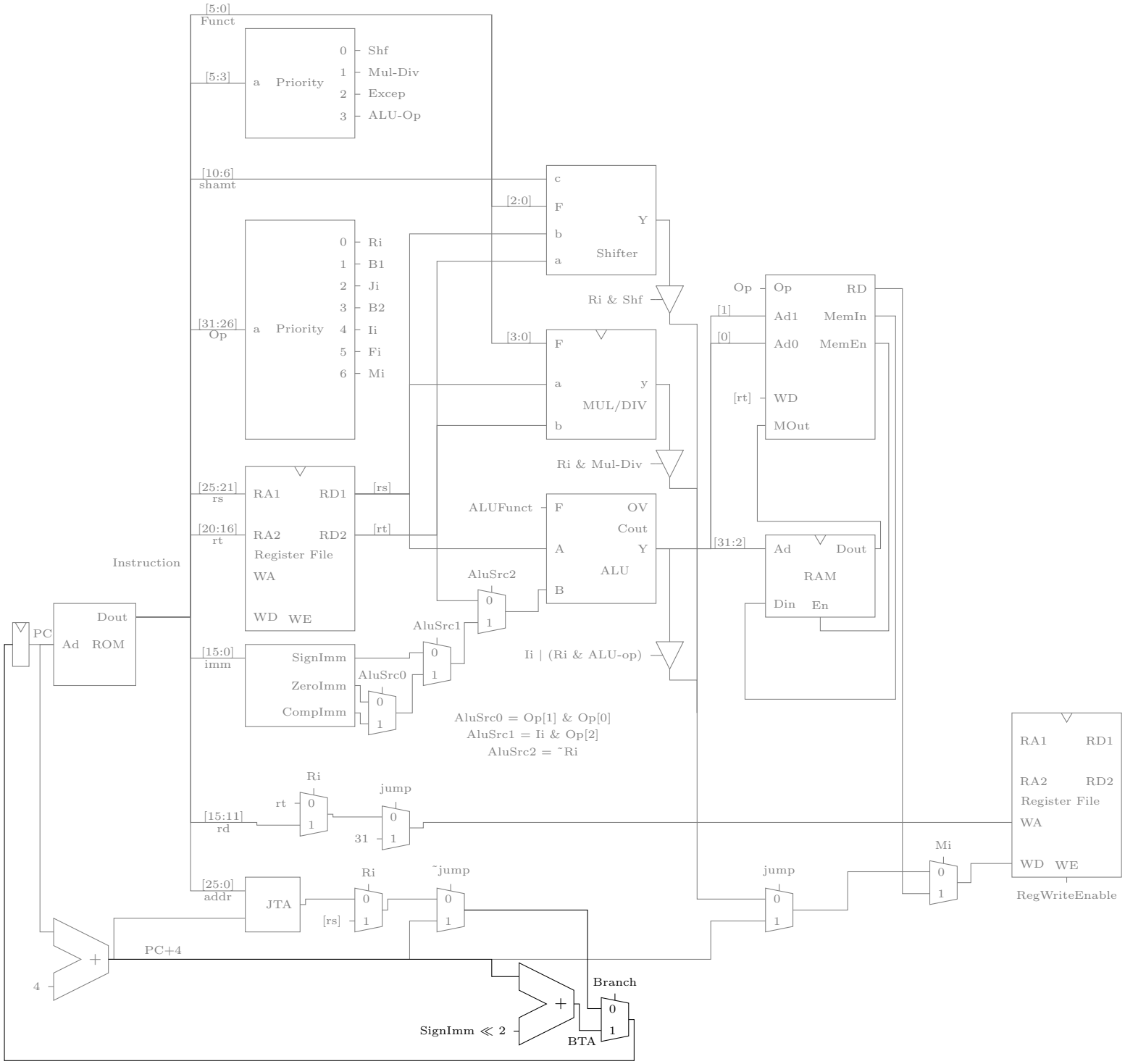

[5:0]
Funct
[5:3]
a
Priority
0
1
2
3
Shf
Mul-Div
Excep
ALU-Op
[10:6]
shamt
c
F
b
a
Shifter
Y
[2:0]
[4:0]
Shf
[3:0]
F
a
b
MUL/DIV
y
Mul-Div
[25:21]
rs
[20:16]
rt
RA1
RD1
RA2
RD2
Register File
WA
WD
WE
[rs]
[rt]
ALUFunct
F
A
B
ALU
OV
Cout
Y
ALU-op
ALUFunct = Funct[3:0]
Instruction
PC
Ad
ROM
Dout
[15:11]
rd
RA1
RD1
RA2
RD2
Register File
WA
WD
WE
PC+4
4
+


[5:0]
Funct
[5:3]
a
Priority
0 Shf
1 Mul-Div
2 Excep
3 ALU-Op
[10:6]
shamt
c
F
b
a
Shifter
Y
[2:0]
Ri & Shf
[31:26]
Op
a
Priority
0 Ri
1 B1
2 Ji
3 B2
4 Ii
5 Fi
6 Mi
[3:0]
F
a
b
MUL/DIV
y
Ri & Mul-Div
[25:21]
rs
[20:16]
rt
RA1
RD1
RA2
RD2
Register File
WA
WD
WE
[rs]
[rt]
ALUFunct
F
OV
Cout
A
Y
ALU
B
AluSrc2
0
1
AluSrc1
0
1
Instruction
PC
Dout
Ad
ROM
[15:0]
imm
SignImm
ZeroImm
CompImm
AluSrc0
0
1
Ii | (Ri & ALU-op)
AluSrc0 = Op[1] & Op[0]
AluSrc1 = Ii & Op[2]
AluSrc2 = ~Ri
Ri
rt
0
1
[15:11]
rd
RA1
RD1
RA2
RD2
Register File
WA
WD
WE
+
PC+4
4


[5:0]
Funct
[5:3]
a
Priority
0
1
2
3
Shf
Mul-Div
Excep
ALU-Op
[10:6]
shamt
c
F
b
a
Shifter
Y
[2:0]
Ri & Shf
[31:26]
Op
a
Priority
0
1
2
3
4
5
6
Ri
B1
Ji
B2
Ii
Fi
Mi
F
a
b
MUL/DIV
y
[3:0]
Ri & Mul-Div
Op
Op
RD
[1]
Ad1
MemIn
[0]
Ad0
MemEn
[rt]
WD
MOut
[25:21]
rs
RA1
RD1
[rs]
[20:16]
rt
RA2
RD2
[rt]
Register File
WA
WD
WE
ALUFunct
F
OV
Cout
A
Y
ALU
B
[31:2]
Ad
Dout
RAM
Din
En
Instruction
PC
Dout
Ad
ROM
AluSrc2
0
1
AluSrc1
0
1
[15:0]
imm
SignImm
ZeroImm
CompImm
AluSrc0
0
1
Ii | (Ri & ALU-op)
AluSrc0 = Op[1] & Op[0]
AluSrc1 = Ii & Op[2]
AluSrc2 = ~Ri
Ri
rt
0
1
[15:11]
rd
RA1
RD1
RA2
RD2
Register File
WA
WD
WE
Mi
0
1
RegWriteEnable
+
PC+4
4


[5:0]
Funct
[5:3]
a Priority
0 Shf
1 Mul-Div
2 Excep
3 ALU-Op
[10:6]
shamt
[2:0]
c
F
b
a
Shifter
Y
Ri & Shf
[31:26]
Op
a Priority
0 Ri
1 B1
2 Ji
3 B2
4 Ii
5 Fi
6 Mi
[3:0]
F
a
b
MUL/DIV
y
Ri & Mul-Div
Op
Op
RD
[1]
Ad1
MemIn
[0]
Ad0
MemEn
[rt]
WD
MOut
[25:21]
rs
RA1
RD1
[rs]
[20:16]
rt
RA2
RD2
[rt]
Register File
WA
WD
WE
ALUFunct
F
OV
Cout
A
Y
ALU
B
[31:2]
Ad
Dout
RAM
Din
En
Instruction
AluSrc2
0
1
AluSrc1
0
1
PC
Dout
Ad
ROM
[15:0]
imm
SignImm
ZeroImm
CompImm
AluSrc0
0
1
Ii | (Ri & ALU-op)
AluSrc0 = Op[1] & Op[0]
AluSrc1 = Ii & Op[2]
AluSrc2 = ~Ri
Ri
rt
0
1
jump
0
1
31
[15:11]
rd
RA1
RD1
RA2
RD2
Register File
WA
WD
WE
RegWriteEnable
Mi
0
1
jump
0
1
+
4
PC+4


[5:0]
Funct
[5:3]
a Priority
0 Shf
1 Mul-Div
2 Excep
3 ALU-Op
[10:6]
shamt
[2:0]
c
F
b
a
Shifter
Y
Ri & Shf
[31:26]
Op
a Priority
0 Ri
1 B1
2 Ji
3 B2
4 Ii
5 Fi
6 Mi
[3:0]
F
a
b
MUL/DIV
y
Ri & Mul-Div
Op
Op
RD
[1]
Ad1
MemIn
[0]
Ad0
MemEn
[rt]
WD
MOut
[25:21]
rs
RA1
RD1
[rs]
[20:16]
rt
RA2
RD2
[rt]
Register File
WA
WD
WE
ALUFunct
F
OV
Cout
A
Y
ALU
B
[31:2]
Ad
Dout
RAM
Din
En
Instruction
PC
Dout
Ad
ROM
AluSrc2
0
1
AluSrc1
0
1
[15:0]
imm
SignImm
ZeroImm
CompImm
AluSrc0
0
1
Ii | (Ri & ALU-op)
AluSrc0 = Op[1] & Op[0]
AluSrc1 = Ii & Op[2]
AluSrc2 = ~Ri
RA1
RD1
RA2
RD2
Register File
WA
WD
WE
RegWriteEnable
Ri
rt
0
1
jump
0
1
31
[15:11]
rd
Mi
0
1
jump
0
1
[25:0]
addr
JTA
Ri
0
1
[rs]
~jump
0
1
PC+4
+
4


[5:0]
Funct
[5:3]
a Priority
0 Shf
1 Mul-Div
2 Excep
3 ALU-Op
[10:6]
shamt
[31:26]
Op
a Priority
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1 B1
2 Ji
3 B2
4 Ii
5 Fi
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[25:21]
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[20:16]
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RA1 RD1
RA2 RD2
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WD WE
[rs]
[rt]
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AluSrc0
AluSrc1
AluSrc2
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Shifter
Ri & Shf
[3:0]
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a
y
MUL/DIV
b
Ri & Mul-Div
ALUFunct
F
OV
Cout
A
Y
ALU
B
Ii | (Ri & ALU-op)
AluSrc0 = Op[1] & Op[0]
AluSrc1 = Ii & Op[2]
AluSrc2 = ~Ri
Op
Op RD
[1]
Ad1 MemIn
[0]
Ad0 MemEn
[rt]
WD
MOut
[31:2]
Ad Dout
RAM
Din En
RA1 RD1
RA2 RD2
Register File
WA
WD WE
RegWriteEnable
Mi
[15:11]
rd
rt
Ri
jump
31
[25:0]
addr
JTA
Ri
[rs]
~jump
jump
PC+4
4
+
Branch
SignImm ≪ 2
BTA