Name :-
ASUID:-

EEE 425/591

ASU Spring 2017

LAB #05

1-bit Adder Design

1. ***Elaborate on your selection of circuit topology***
insert caption here

Schematic View

**insert procedure used here*

Delay Optimization/Sizing

Device Names	Value (nm)

⋮

2. **insert plots here*

Delay Measurement plots for TT Corner

Delay Measurements for 5 Corners

	TT	SS	SF	FS	FF
A→S					
A→Cout					
B→S					
B→Cout					
Cin→S					
Cin→Cout					

3. ** insert caption here*

Layout View

**insert plots here*

Delay Measurement plots for TT Corner

Delay Measurements for 5 Corners

	TT	SS	SF	FS	FF
A→S					
A→Cout					
B→S					
B→Cout					
Cin→S					
Cin→Cout					

Name :-
ASUID:-

**insert captions here*

Layout & LVS Pass

4. **insert procedure here*

EDP and Area

Delay (Max. for TT corner)	Energy (TT corner)	Energy Delay Product	Area